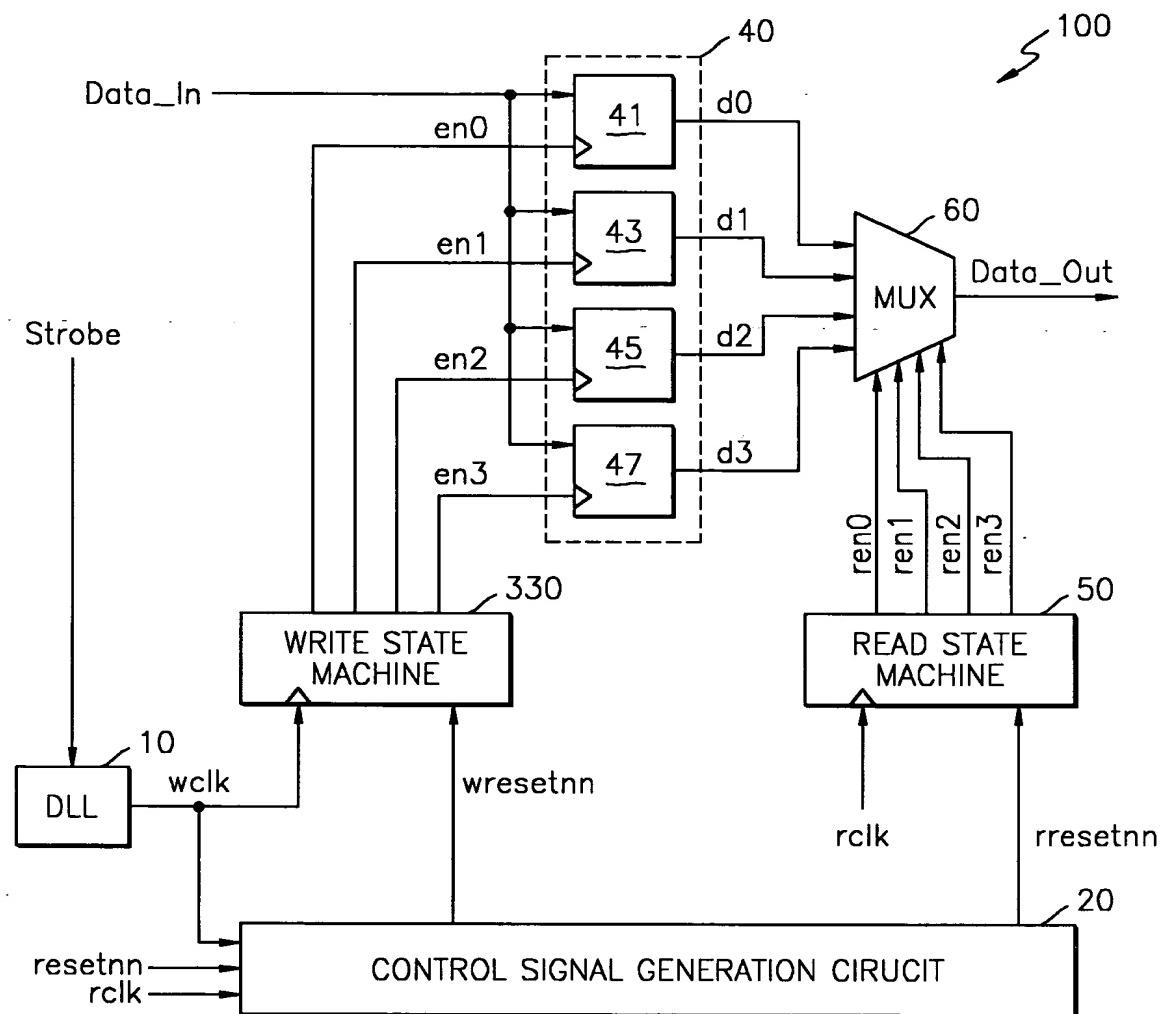


CONTROL SIGNAL GENERATION CIRCUIT AND DATA TRANSMISSION CIRCUIT HAVING  
THE SAME

Application No. [NEW] – Attorney Docket No. SEC.1072  
Inventors: Jae-Kwan KIM et al.

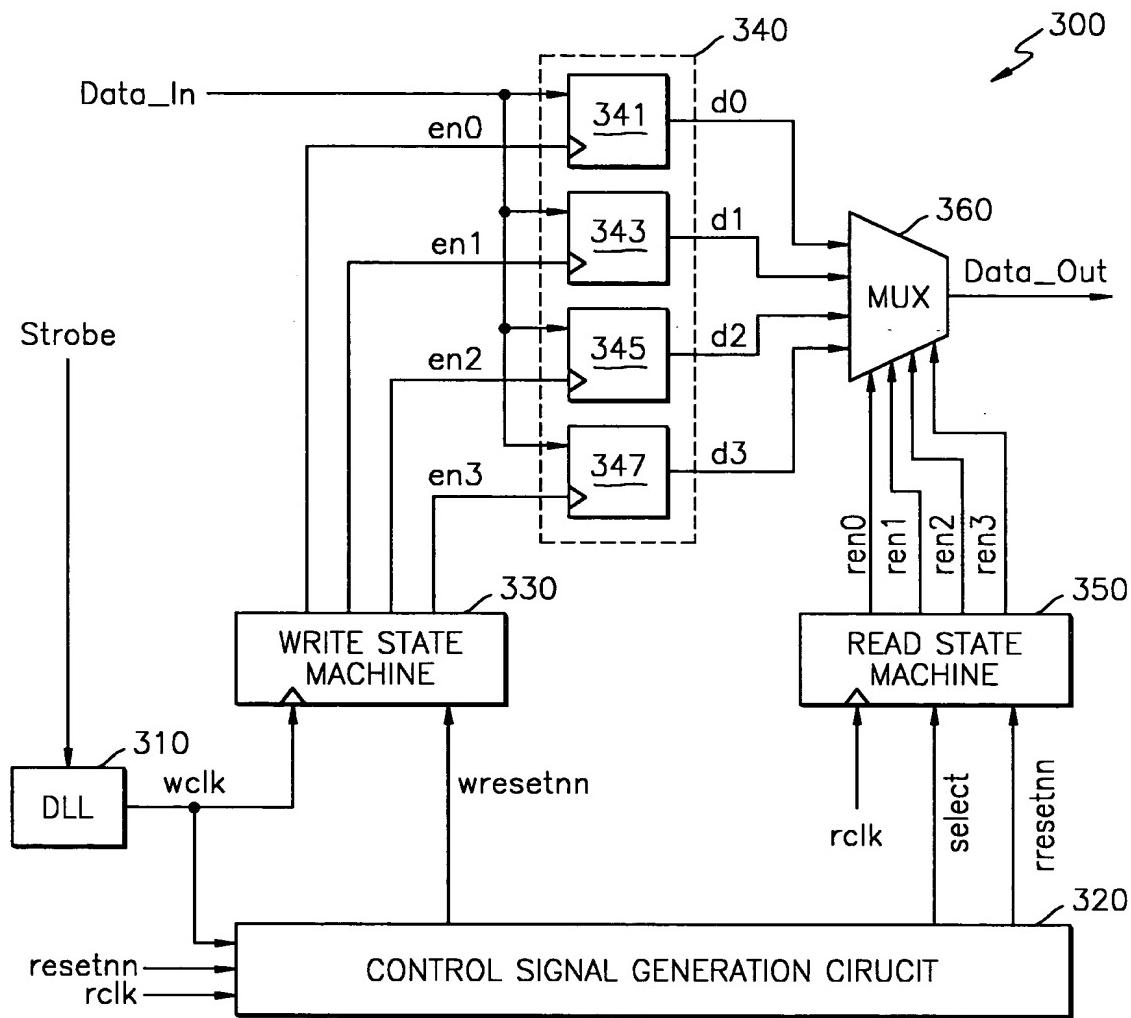
FIG. 1



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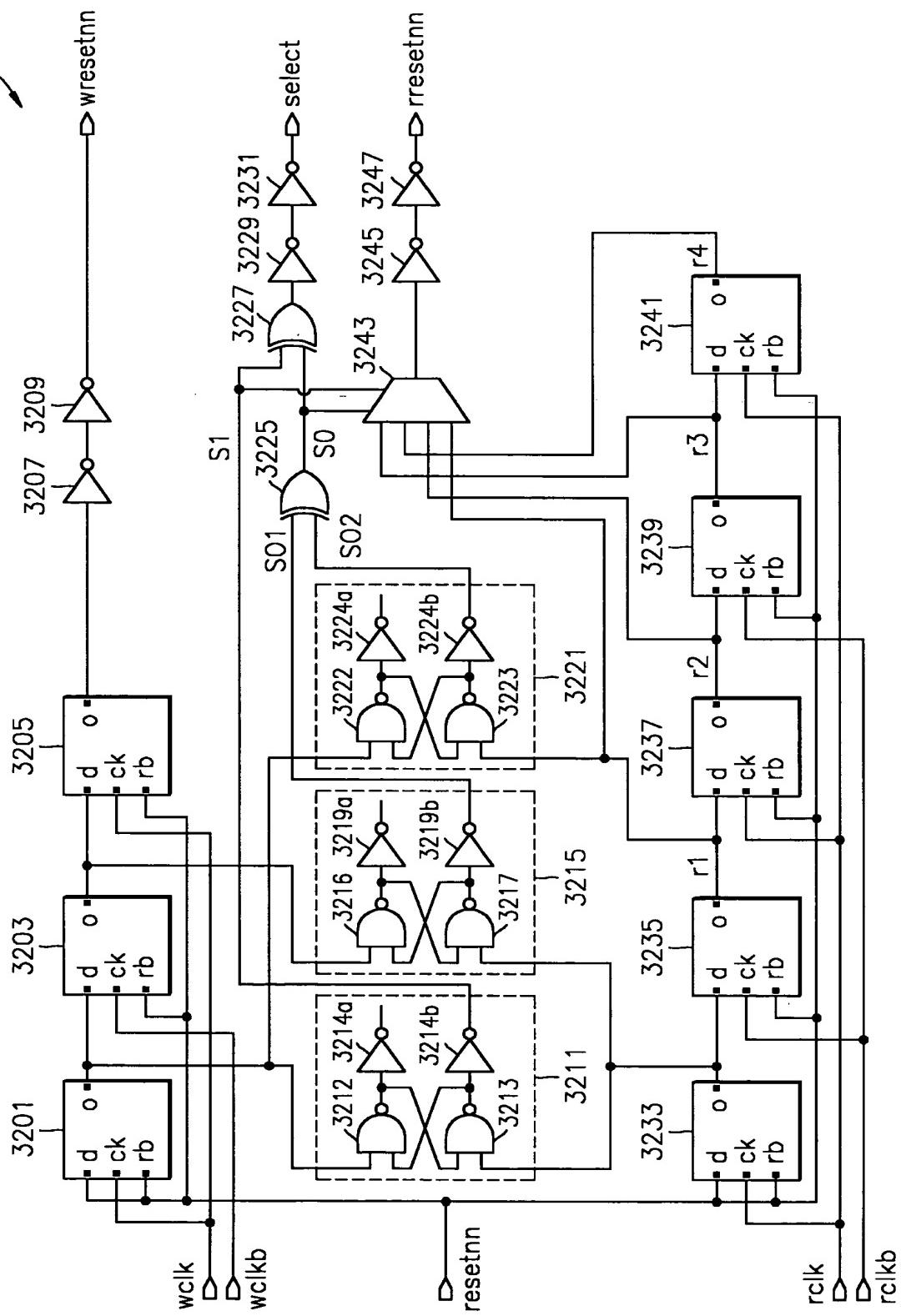
FIG. 2



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FIG. 3



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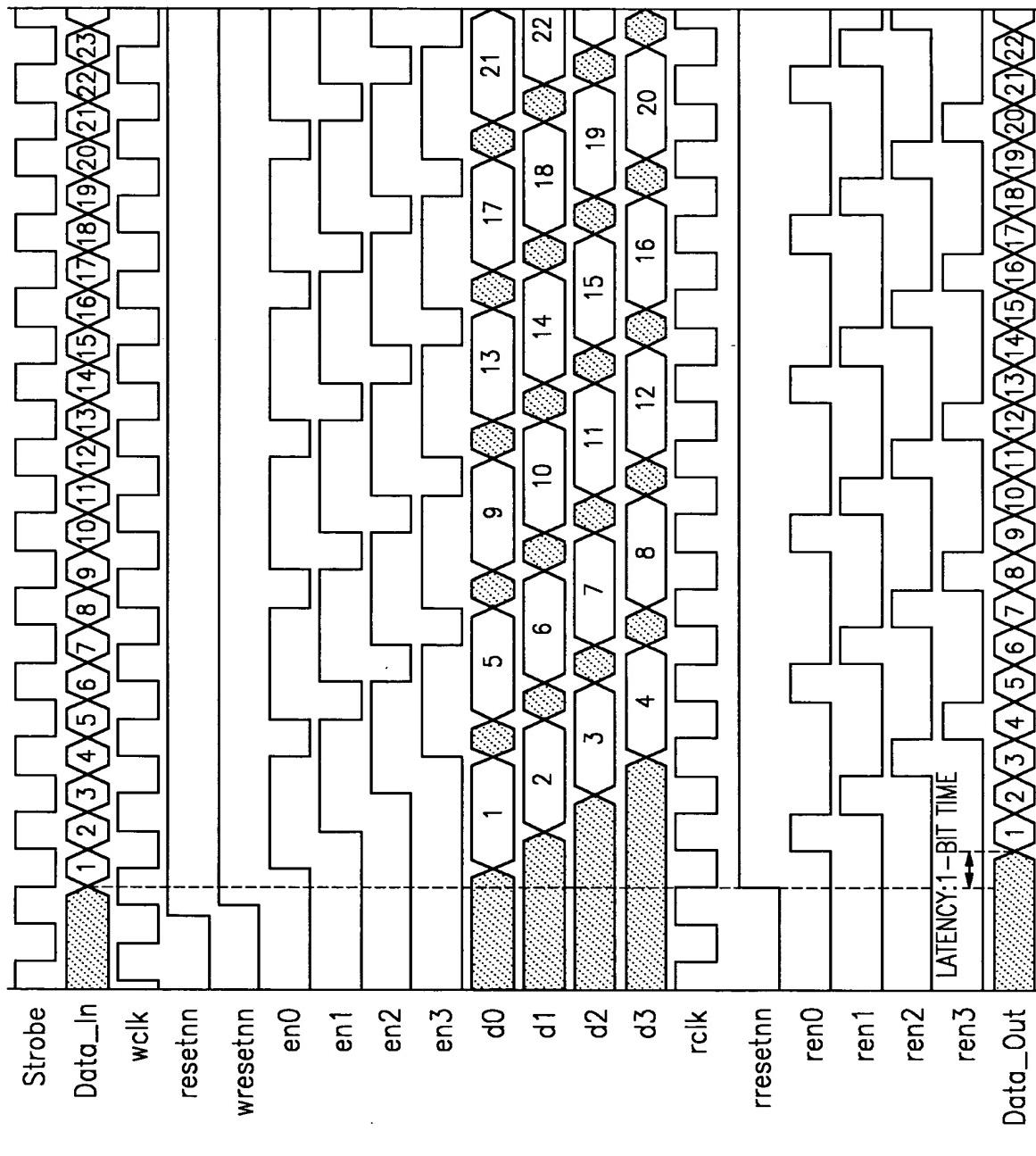


FIG. 4

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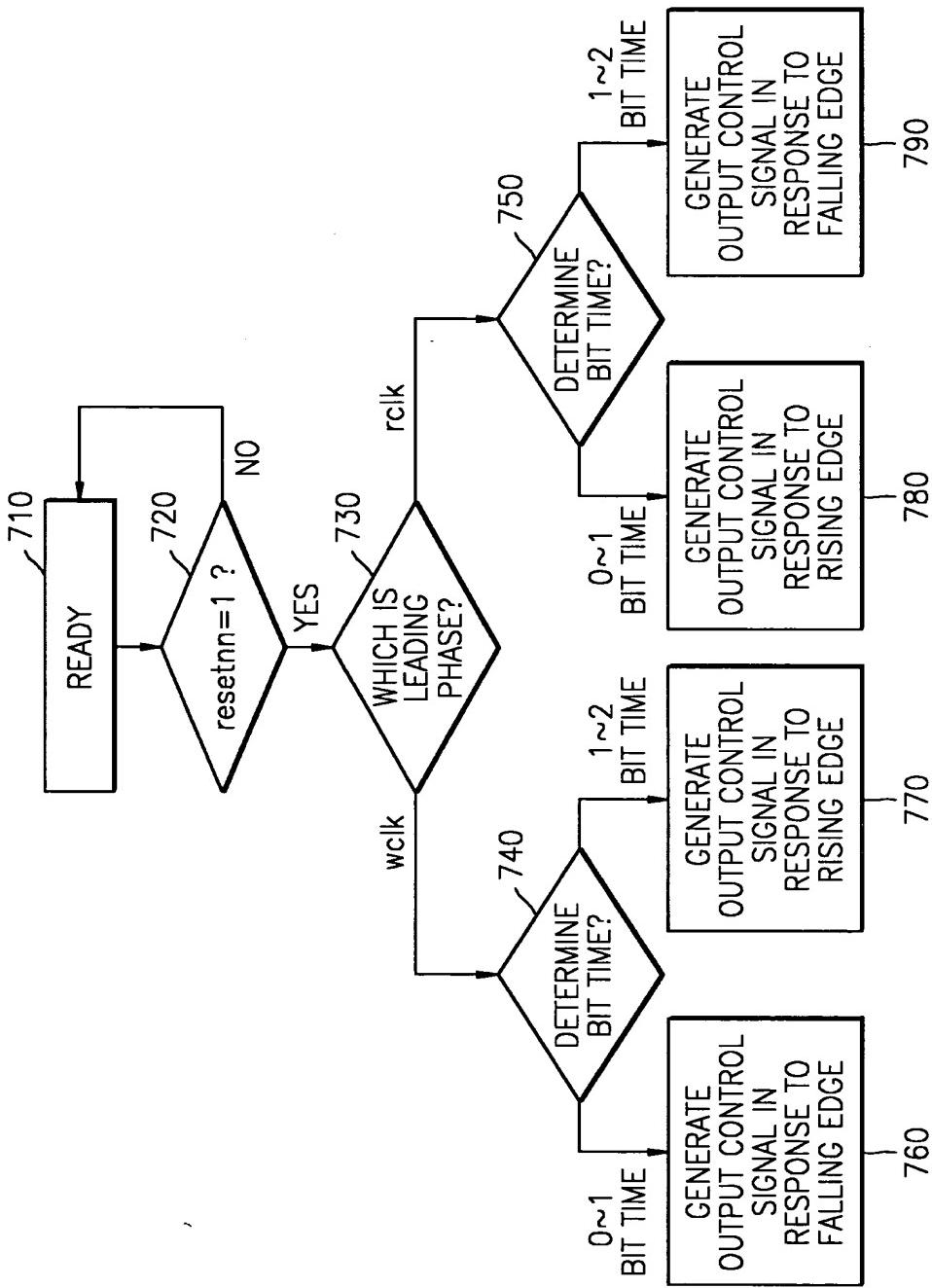
FIG. 5

LEAD	DELAY (BIT TIME)	s1	s01	s02	s0	rresetnn	SELECT
wclk	0~1	0	1	0	1	r2	FALLING EDGE
	1~2	0	0	0	0	r1	RISING EDGE
rclk	0~1	1	1	0	1	r3	RISING EDGE
	1~2	1	1	1	0	r4	FALLING EDGE

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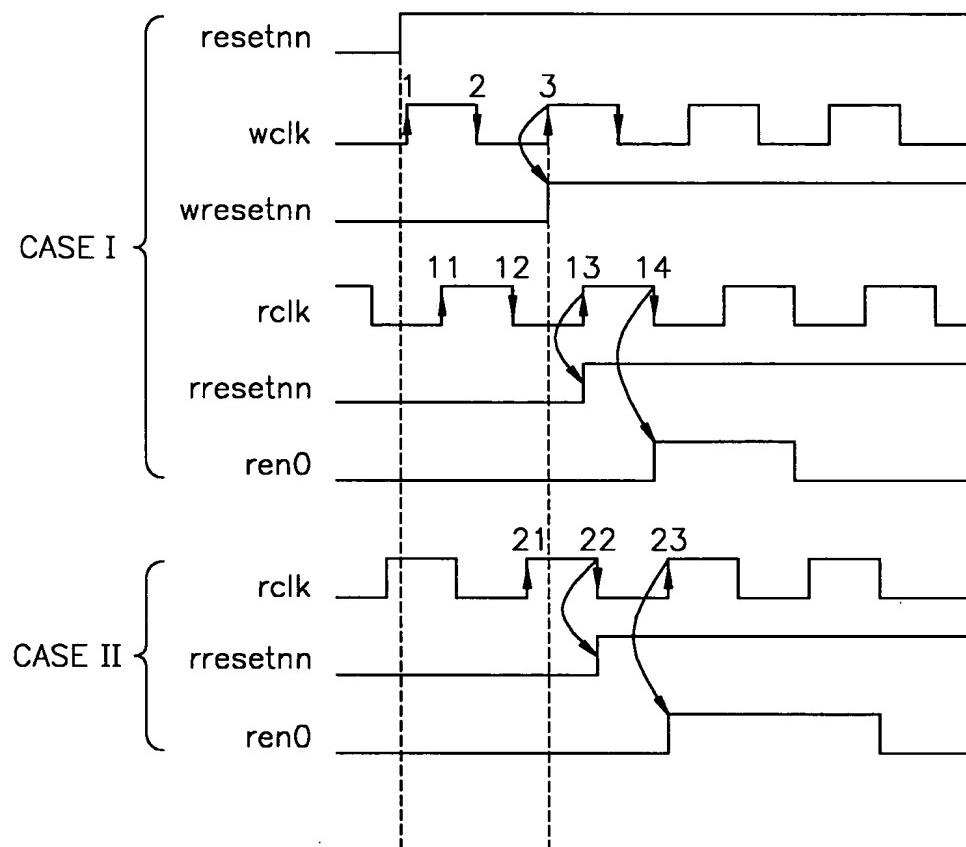
FIG. 6



CONTROL SIGNAL GENERATION CIRCUIT AND DATA TRANSMISSION CIRCUIT HAVING  
THE SAME

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FIG. 7



CONTROL SIGNAL GENERATION CIRCUIT AND DATA TRANSMISSION CIRCUIT HAVING  
THE SAME

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FIG. 8

